In the Claims:

Claims 1-30 (canceled).

Claim 31 (currently amended): A silicon integrated circuit fabricated using a method of removing excess interconnect material during fabrication of said silicon integrated circuit, said method of removing comprising the steps of:

dispensing a slurry including abrasive particles and chemical on a sample having said excess interconnect material;

polishing said sample with said slurry, using a polishing pad having a plurality of pits, to remove said excess interconnect material, wherein said abrasive particles and chemical become embedded into said plurality of pits of said polishing pad;

reducing said dispensing of said slurry after said polishing for a first period of time, wherein said dispensing of said slurry is reduced to a stop; and

polishing said sample using said polishing pad for a second period of time to remove said excess interconnect material.

Claim 32 (canceled).

Claim 33 (previously presented): The silicon integrated circuit of claim 31, wherein said silicon integrated circuit includes a metal gate fabricated with Atomic Layer Deposition (ALD) and said excess interconnect material is copper.

Claim 34 (previously presented): The silicon integrated circuit of claim 33, wherein said ALD includes Ta.

Claim 35 (previously presented): The silicon integrated circuit of claim 31, wherein said step of reducing occurs after a step of endpoint detection of said step of polishing said sample with said slurry, based on a thickness of said excess interconnect material.

Claim 36 (previously presented): The silicon integrated circuit of claim 35, wherein said thickness of said excess interconnect material is determined based on optical reflectivity.

Claim 37 (previously presented): The silicon integrated circuit of claim 31, said excess interconnect material is copper.

Claim 38 (previously presented): The silicon integrated circuit of claim 31, wherein said plurality of pits are created by abrading a polishing surface of said polishing pad with an abrasive disc.

Claim 39 (previously presented): The silicon integrated circuit of claim 31, wherein said steps of polishing are performed at a pressure of about 1.5 psi.

Claim 40 (previously presented): The silicon integrated circuit of claim 31, wherein said steps of polishing are performed at a pressure of about 2.7 psi.